AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) A semiconductor component with trench isolation for defining active regions in a semiconductor substrate, the trench isolation comprising:

a deep isolation trench with a first covering insulation layer below a surface of the semiconductor substrate and a second covering insulation layer over the first covering insulation layer and above the surface of the semiconductor substrate, a gate oxide layer over a surface of the second covering insulation layer, a side wall insulation layer, an electrically conductive filling layer, which is electrically connected to a predetermined doping region of the semiconductor substrate in a bottom region of the isolation trench, and wherein the first covering insulation layer is over a top surface of the electrically conductive filling layer; and

further comprising:

a trench contact, which comprises:

a deep contact trench with a side wall insulation layer and an electrically conductive filling layer which is electrically, contact-connected to the predetermined doping region of the semiconductor substrate in a bottom region of the contact trench;

a trench contact insulation layer above a surface of the electrically conductive filling layer; and

a contact opening through the trench contact insulation layer and in contact with a top surface of the electrically conductive filling layer, and

wherein a composition of the electrically conductive filling layer that is electrically, contact-connected to the predetermined doping region of the semiconductor substrate in a bottom region of the contact trench is the same as a composition of the electrically conductive filling layer having a top surface in contact with the contact opening.

2. (Previously presented) The semiconductor component of claim 1, wherein the first covering insulation layer is within the isolation trench.

3. (Previously Presented) The semiconductor component of claim 1, wherein the trench isolation and the trench contact have a larger depth than an associated depletion zone in the semiconductor substrate.

4. (Previously Presented) The semiconductor component of claim 1, wherein the trench isolation further comprises a widened, shallow isolation trench at a surface of the semiconductor substrate configured for filling non-active regions.

5. (Previously Presented) The semiconductor component of claim 1, wherein the predetermined doping region comprises a doping well comprising a multiple well structure.

6. (Previously Presented) The semiconductor component of claim 1, wherein the semiconductor substrate comprises Si, the second covering insulation layer and side wall insulation layer comprise SiO_2, and the electrically conductive filling layer comprises highly doped polysilicon.

7. (Withdrawn) A method for fabricating a semiconductor component having trench isolation comprising: a) preparing a semiconductor substrate having at least one predetermined doping region; b) forming deep trenches to the predetermined doping region configured for at least one trench isolation and a trench contact; c) forming a side wall insulation layer on the side walls of the deep trenches; d) forming an electrically conductive filling layer in the deep trenches; e) removing at least the

electrically conductive filling layer in the upper region of the trenches for the at least one trench isolation to form shallow trenches; and f) forming a covering insulation layer in the shallow trenches of the trench isolation.

8. (Withdrawn) The method of claim 7, wherein, preparing a semiconductor substrate having at least one predetermined doping region comprises forming one of a double or triple well structure in the semiconductor substrate.

9. (Withdrawn) The method of claim 7, wherein forming deep trenches comprises forming a first hard mask layer and anisotropically etching the semiconductor substrate.

10. (Withdrawn) The method of claim 7, wherein forming a side wall insulation layer comprises thermal oxidation to form a trench insulation layer and anisotropically etching the trench insulation layer to remove a bottom region of the trench insulation layer.

11. (Withdrawn) The method of claim 7, wherein forming an electrically conductive filling layer comprises forming a highly doped semiconductor material having the same conduction type as the predetermined doping region.

12. (Withdrawn) The method of claim 7, wherein in step e), forming shallow trenches further comprises removing the side wall insulation layer and adjoining regions of the semiconductor substrate in the upper region of the deep trenches to form widened trench isolation structures.

13. (Withdrawn) The method of claim 7, wherein forming shallow trenches comprises removing only the conductive filling layer with or without the side wall insulation layer in the upper region of the trenches to form narrow trench isolation structures.

14. (Withdrawn) The method of claim 7, wherein forming a covering insulation layer comprises one of oxidizing to form a first covering insulation partial layer depositing to form a second covering insulation partial layer in the shallow trench, or both oxidizing and depositing.

15. (Canceled)